High Frequency CCII Based Ameliorated Band-Pass Filter

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Abstract— In this paper, a grounding capacitance multiplier is presented. This block is very important because he presents a better solution to resolve the problems occurred by the integration of high capacitance value or the problem of tuning that value of the capacitance. We emphasize the fact that the presented applications are well suited for integration since their value can be tuned by simple action on their bias current. Implementations of these topologies based on an improved high frequency translinear CCII were done. The grounding capacitance multiplier has a variable value tunable in the range [53pF-83pF] by varying a dc current between 10µA and 400µA. Moreover, one based current mode ameliorated band pass filter are implemented. The current mode filter has a tunable central frequency in the range [745MHz-1.08GHz].

Keywords— Translinear Current Conveyor; Grounding Capacitance Multiplier; Ameliorated Current Mode Band Pass-filter

I. INTRODUCTION

It is well known that the integration of capacitances larger than 50pF is not desirable because of the occupied area and the noise effect provoked by these values. In some application is necessary to vary the value of the capacitance or to have higher capacitive value. A possible solution is the use of capacitance multiplier. Recently, an active capacitive multiplier has been developed by used the second generation current conveyor [1,2].

Second generation Current Conveyor (CCII) is a basic building block of frequency function circuit design. It adds a tremendous simplification of such designs since it can be modelled by simple asymptotic input-output relations. Since their introduction in 1970 [3], the use of CCII is more and more generalized in filters and oscillators design. Owing to their extra modularity, current controlled design features was achieved. Such control is of great importance, namely in telecommunication applications. A lot of varieties of CCII electronic implementations were proposed, having as motivation power supply reduction and high frequency operations. However proposed CMOS CCII based applications does not resolve the high frequency limitations. Recently, in CMOS process, current mode circuits have seen a tremendous increasing of the frequency response. Extrapolating these performances to CCII based circuits is still open [4].

The paper is organized as follows: in section II, we present a transistor level implementation of the CCII that we apply in the above proposed applications [5]. In section III, CCII based grounding capacitance multiplier are presented. An ameliorated controllable current mode band pass filter is proposed. Simulation results using the CCII for the different applications are presented.

II. Current conveyor

Fig. 1 shows a general representation of CCII. It is a three terminal block that ensures two functionalities between its terminals:

- A Current conveying between terminals X and Z.
- A Voltage follower between terminals X and Y.

![Fig. 1 General Representation of CCII](image)

Thus, in order to get nearly ideal transfers, a CCII should be characterized by low impedance on terminal X and high impedance on terminals Y and Z.

The CCII behaviour taking into account parasitic impedances is given by the following relation:

\[
\begin{align*}
\begin{bmatrix}
I_x \\
V_x \\
I_z
\end{bmatrix} &= \begin{bmatrix}
\frac{1}{R_{x} + \frac{1}{C_{x}}} & 0 & 0 \\
\frac{1}{R_{y} + \frac{1}{C_{y}}} & 0 & \frac{1}{R_{z} + \frac{1}{C_{z}}} \\
0 & \frac{1}{R_{y} + \frac{1}{C_{y}}} & 0
\end{bmatrix}
\begin{bmatrix}
V_x \\
I_x \\
V_z
\end{bmatrix}
\end{align*}
\]

(1)

where and are current and voltage transfers of the CCII. RY, CY and RZ,CZ are parasitic resistances on port Y and Z respectively, they are ideally infinite impedances. Rx is the parasitic resistance at port X being ideally a short circuit.

In [6], the basic translinear configuration was considered for improvement. A new signal path is introduced for the current conveying, speeding up its transfer and reducing the parasitic impedance on port X.
This improved translinear based configuration is depicted in Fig.2[6]. The corresponding optimum device scalings [4] are dressed in table 1, where MNxx and MPxx refer to PMOS and NMOS mirror transistor and xx is the index of the different transistors. The main performances of this structure are summarized in table 2.

![Fig. 2 Improved configuration of translinear based CCII](image)

### Table 1 MOS transistor geometry

<table>
<thead>
<tr>
<th>Device Name</th>
<th>Aspect ratio W/L (µm)</th>
</tr>
</thead>
<tbody>
<tr>
<td>M1, M2</td>
<td>12/0.35</td>
</tr>
<tr>
<td>M3, M4</td>
<td>36/0.35</td>
</tr>
<tr>
<td>M_{pxx} (in PMOS current mirrors)</td>
<td>18/0.35</td>
</tr>
<tr>
<td>M_{nxx} (in NMOS current mirrors)</td>
<td>6/0.35</td>
</tr>
</tbody>
</table>

### Table 2 Basic characteristics of the improved translinear based CCII+ (with \(I_0=100\mu A\) and ±2.5V as supply voltage)

<table>
<thead>
<tr>
<th>Parameter</th>
<th>Obtained results</th>
</tr>
</thead>
<tbody>
<tr>
<td>(\beta)</td>
<td>0.96</td>
</tr>
<tr>
<td>(\alpha)</td>
<td>0.972</td>
</tr>
<tr>
<td>(F_{CI})</td>
<td>2.6GHz</td>
</tr>
<tr>
<td>(F_{CV})</td>
<td>3.9GHz</td>
</tr>
<tr>
<td>((R_Y/C_Y))</td>
<td>25.25kΩ/49fF</td>
</tr>
<tr>
<td>((R_Z/C_Z))</td>
<td>34.5kΩ/9.45fF</td>
</tr>
<tr>
<td>(R_X)</td>
<td>19Ω</td>
</tr>
</tbody>
</table>

The corresponding input parasitic resistance at port X is shown in eqn (2)

\[
R_X = \frac{1}{g_m A_2} + \frac{1}{g_{m5} A_4} \quad (2)
\]

Where \(A_i\) is the voltage gain: \(A_i = (1+g_{m0}r_o)\), \(r_o = 4.2\), where \(g_{m0}\) and \(r_o\) are respectively the transconductance and output resistance of transistor M2.

\[
g_{m0} = \sqrt{2K \left( \frac{W}{L} \right) (1 + \frac{AV_{DS}}{A_0}) I_0}
\]

\[
r_o = \frac{1 + AV_{DS}}{A_0}
\]

Fig. 3 shows simulated values of RX versus \(I_0\). We can see that this resistance can be controlled between 11.8 and 30.47 by simply varying current controls in the range of [1µA-400µA]. We emphasize the fact that this structure presents a very lower parasitic resistance at X port.

![Fig. 3 The RX versus control current](image)

### III. Current Mode Filter

To realise the current mode filter it’s necessary to use the capacitance element. But one of the most limiting problems in the design of integrated circuits is constituted by the realization of high valued capacitors, which have the heavy drawback of high occupation of silicon area. Moreover, in some sensor applications, it can be useful to deal with capacitance values higher than those normally given by capacitive sensors. In these cases, the use of capacitance multipliers can be very important. In this paper, we present to structure of capacitance multipliers. These structures of capacitance multipliers are used to ameliorate the Current Mode Selective Filter.

### IV. A grounding capacitance multiplier:

Fig. 4 [2] shows the circuit diagram for the capacitance multiplication using current conveyors followed by a current amplifier A. This capacitance multiplier uses one positive-type and one negative-type second-generation current controlled conveyors and three passive elements. It can be shown that the ideal input capacitance is given by:

\[
C_I = A \cdot C_1
\]

![Fig. 4 A grounding capacitance multiplier](image)

\[
V_{y1} = R_2 \cdot I_{out1} = V_{x1} = R_1 \cdot I_{x1} = -R_1 \cdot I_{out2}
\]

Or:

\[
V_{in} = V_{x2} = I_{x2} \cdot (s \cdot C_1) = -I_{out1}/(s \cdot C_1) = -R_1 \cdot I_{out2}/(s \cdot C_1 \cdot R_2)
\]

From above equations we conclude that:

\[
I_{out2} = (R_2/R_1) \cdot I_{out1}
\]

And:

\[
I_{out2} = -I_{in}
\]
\[ C_f = \frac{R_2}{R_1} \cdot C_1 \]  

\[ (6) \]

A. Simulated Results

In the reality \[ C_f = \frac{R_2}{(R_1 + R_{eq})} \cdot C_1 \] . Showing this relation we conclude that the \( C_f \) can be tuned from \( R_{X1} \) (for example if \( I_{o1} = 100 \mu A \) the \( C_f = 84 \text{pF} \)).

The grounding capacitance multiplier shown at figure 9 is simulated using Pspice software for \( C_1 = 10 \text{pF} \). Simulation results are shown in Fig. 5. When varying the control current \( I_{o1} \) (having \( R_1 = 100 \Omega, R_2 = 1 \text{K} \Omega \)) between 10 and 400, \( C_f \) is tuned in the range \([53 \text{pF}-83.8 \text{pF}]\).

Fig. 5 Tuning of the \( C_f \) with varying \( I_{o1} \)

V. Current Mode Selective Filter

Two topologies are used to implement second order active filters employing current conveyors. One is based upon using simulated inductance \([7]\). While the other is obtained by modified this one \([3,8]\).

A. Current-Controlled Active inductance

The architecture of the grounded inductance is giving in Fig. 6. Where the value of this inductance is given by

\[ L = R_{X1}R_{X2}C \]  

\[ (7) \]

A-Implementation from two \( \text{CCCII}^+ \)  

B- Equivalent circuit

Fig. 6 Implementation of the non ideal inductance \( \text{CCCII}^+ \)

B. Current Mode selective filter

A Negative resistor is used to compensate \( R \), to cancel the effects of the parasitic shunt resistors (\( R_{X1} \) and \( R_{X2} \)). This structure is shown in fig. 7 \([3]\).

Now connected a capacitor with the non ideal inductance and the Negative resistor to realised a design equivalent to a shunt RLC circuit. The second order band pass filter is showing in fig. 8.

When the \( \text{CCCII1}, \text{CCCII2} \) and \( C_1 \) implement the non ideal inductance, \( C \) is the shunt capacitor. The \( \text{CCCII3} \) as a controlled negative resistance is used to cancel the effects of the parasitic shunt resistors (\( R_{X1} \) and \( R_{X2} \)). Finally the output current signal is obtained through \( \text{CCCII4} \).

The transfer function of the filter shown in figure is giving by:

\[ H(s) \cdot \frac{I_{out}}{I_{int}} = \frac{\frac{s}{R_{eq} R_C C_5}}{\frac{s^2}{C_2 R_{eq}} + 1} \cdot \frac{1}{L C_2} \]  

\[ (8) \]

Where \[ \frac{1}{R_{eq}} = \frac{1}{R_1} + \frac{1}{R_2} + \frac{1}{R_3} \cdot \frac{1}{R_3} \cdot \frac{1}{R_3} \cdot \frac{1}{R_3} \cdot \frac{1}{R_3} \].

Its characteristic parameters are the following:

\[ W_0 = \frac{1}{\sqrt{R_1 R_2 C_1 C_2}} \]  

\[ (9) \]

\[ Q = \frac{R_{eq}}{\sqrt{R_1 R_2 \cdot C_2}} \cdot \frac{C_2}{C_1} \]  

\[ (10) \]

In this circuit the center frequency can be adjusted independently of the Q-factor with \( C_1 \cdot C_2 \) if the ratio \( C_1 \) is left constant. And the Q-factor can be tuned from \( R_{X3} \) or \( R_{X4} \) (\( I_{o3} \) or \( I_{o4} \)) without changing the center frequency.

It's desirable to adjust the center frequency after integration. For this reason it is not allowed to change the capacitor’s values. For this reason we present in Figure 9 the ameliorate Current Mode Selective Filter.
The transfer function of the ameliorated filter shown in figure is given by:

\[ H(s) = \frac{I_{out}}{I_{int}} = \frac{R_2 R_4 C_2}{R_1 C R_3 R_5 + R_1 L R C} \]  

(11)

Its characteristic parameters are the following:

\[ W_0 = \frac{R_1}{R_2 R_3 R_4 R_5 C} \]  

(12)

\[ Q = \frac{R e q}{R_2 R_3 R_4} \sqrt{\frac{C_2}{C_1}} \]  

(13)

C. Simulated Results

The proposed filter is simulated using Pspice for different CCII bias currents. Simulation results are shown in Fig.10 When varying the control current \( I_{o8} \) between 10\( \mu \)A and 400\( \mu \)A, the central frequency is tuned in the range [745MHz-1.08GHz] (\( I_{o1}=100\mu A, I_{o2}=250\mu A, I_{o4}=170\mu A, I_{o3}=10\mu A, I_{o5}=I_{o6}=I_{o7}=100\mu A \)).

![Fig. 9 The ameliorated Current-Mode Second Order Bandpass Filter](image)

The proposed circuit is verified through PSPICE simulation with promising results.

REFERENCES


Achwek Ben Saied was born in 1981 in Sfax, Tunisia. He received the electrical engineering degree in 2005 and Master degree on electronics and communication in 2006, both from the National School of Engineering of Sfax (ENIS), Tunisia. He is currently working toward the Ph.D. degree in Electronic at the same school. His research interest is to design RF integrated circuit for wireless communication transceivers, especially the design of active RF oscillator and filter for front end receiver.

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Dorra Sellami Masmoudi was born in Sfax, Tunisia in 1969. She received the degree of engineering from Sfax National Engineering School in 1994 and has been awarded by the president of the republic of Tunisia. Subsequently she joined I.X.L. laboratory of Microelectronics at Bordeaux and received her Ph.D. degree in 1998 in electronics system design and she has been assistant Professor at Sfax National Engineering School from 1999. At 2006, Dorra Sellami Masmoudi gets HLR degree. Her research includes low-voltage low-power design, analog and digital neural network network implementation and image processing for pattern recognition.

VI. Conclusion

In this paper, a new current-Mode Second Order Bandpass filter circuit based on CCII’s and grounding capacitance multiplier is presented. Frequency of the filter can be varied by varying the value of the active-capacitance. The capacitive value can be widely adjusted by any input bias currents of the CCII. The proposed circuit is verified through PSPICE simulation with promising results.

Fig. 10 Tuning of the Q-factor and central frequency with varying \( I_{o8} \)